2811

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	78

Application Number	09/915,160
Filing Date	July 25, 2005
First Named Inventor	Toshiharu YANAGIDA
Art Unit	2811
Examiner Name	Junghwa M. Im
Attorney Docket Number	9792909-5171

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
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- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
  - Certified translation of the two priority documents
  - Return receipt postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Sonnenschein Nath & Rosenthal LLP		
Signature	M D Murray		
Printed name	Mickki D. Murray		
Date	September 1, 2005	Reg. No.	56,846

CERTIFICATE OF TRANSMISSION/MAILING

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Signature	Valerie Tomlinson		
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S99P1000**01

(1)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Toshiharu YANAGIDA, Tokyo, Japan

APPLICATION NO.: 09/915,160 Group Art Unit: 2811

FILING DATE: July 25, 2001 Examiner: Junghwa M. Im

TITLE: SEMICONDUCTOR APPARATUS AND PROCESS OF PRODUCTION THEREOF

Hon. Commissioner for Patents,
P.O. Box 1450 Alexandeia, VA 22313-1450

SIR;

CERTIFIED TRANSLATION

I, Mariko YOSHIDA, am an official translator of the Japanese language into the English language and I hereby certify that the attached comprises an accurate translation into English of Japanese Application No. H10-247393, filed on September 1, 1998.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

29 Aug 2005

Mariko Yoshida

Date Mariko YOSHIDA

[Name of Document] Request for Patent

[Management No. used by Applicant] 9800686602

[Filing Date] Sptember 1, 1998

[Filing to] Director-General of Patent Office

[IPC] H01L 23/00

[Name of Invention] Solder Bumps And Method Of Producing The Same

[Number of Claims] 10

[Inventor]

[Domicile or Residence] c/o SONY CORPORATION, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, Japan

[Name] Toshiharu YANAGIDA

[Applicant]

[Identification No.] 000002185

[Name] SONY CORPORATION

[Name of Representative] Nobuyuki IDEI

[Attorney]

[Identification No.] 100096806

[Attorney]

[Name] Shintaro OKAZAKI

[Phone Number] +81-3-3264-4811

[Assigned Attorney]

[Identification No.] 100098796

[Attorney]

[Name] Akira ARAI

[Phone Number] +81-3-3264-4811

[Indication of Official Fee]

[Prepaid Note. No.] 029676

[Fee(Yen)] 21,000

[List of Submitted Objects]

[Name of Object] Specification 1

[Name of Object] Drawings 1

[Name of Object] Summary 1

[No. of General-Authorization] 9709207

[Proof] Yes

[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION] Solder Bumps And Method Of Producing The Same

[CLAIMS]

[Claim 1]

A solder bumps comprising:

solder ball bumps formed on electrode pads of a semiconductor device and

a resin filled on a surface of a pad side of the semiconductor device so as to surround a side surface of the solder ball bumps,

surfaces of the solder ball bumps projecting out from the resin being cleaned by plasma cleaning.

[Claim 2]

A solder bumps as set forth in claim 1, wherein the solder ball bumps are first solder ball bumps and second solder ball bumps different composition from the first solder ball bumps and to be brought into contact with solder precoated to a connecting land of a printed circuit board is included on the first solder ball bumps at least in a vertical direction of the electrode pad.

[Claim 3]

A solder bumps as set forth in claim 2, wherein the first solder ball bumps are comprised of high melting point solder and the second solder ball bumps are

comprised of eutectic solder.

[Claim 4]

A method of producing solder bumps comprising:

a first step of forming solder ball bumps on electric pads of a semiconductor device;

a second step of filling a resin on a surface of the electrode pad side of the semiconductor device so as to surround a side surface of the solder ball bumps; and

a third step of cleaning surfaces of the solder ball bumps projecting out from the resin by plasma cleaning.

[Claim 5]

A method of producing solder bumps as set forth in claim 4, wherein the plasma cleaning in the third step is at least sputter etching by discharge plasma of an inert gas.

[Claim 6]

A method of producing solder bumps as set forth in claim 4, wherein the plasma cleaning in the third step is at least oxygen plasma treatment and then sputter etching by discharge plasma of an inert gas.

[Claim 7]

A method of producing solder bumps as set forth in claim 4, wherein the plasma cleaning in the third step is at least oxygen plasma treatment and then sputter etching

by discharge plasma of a reducing gas.

[Claim 8]

A method of producing solder bumps as set forth in claim 4, after the third step, further comprises a fourth step of forming second solder ball bumps, which is different in composition from the first solder ball bumps and to be brought into contact with solder precoated to a connecting land of a printed circuit board, on the surfaces of the first solder ball bumps serving as the solder ball bumps at least in a vertical direction of the electrode pad.

[Claim 9]

A method of producing solder bumps as set forth in claim 8, wherein the first solder ball bumps are comprised of high melting point solder and the second solder ball bumps are comprised of eutectic solder.

[Claim 10]

A method of producing solder bumps as set forth in claim 4, wherein the respective steps up to at least the third step is performed to a semiconductor device formed on a semiconductor substrate in a semiconductor wafer state.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to solder bumps formed on a connecting terminal portion of a semiconductor substrate to mount a semiconductor IC or other semiconductor device and a method of producing the same.

[0002]

[Prior Art]

In recent years, digital video cameras, digital cellular phones, notebook-type personal computers, and other portable electronic equipment have spread widely. There are mounting demands for reducing the size, reducing the thickness, and reducing the weight of these portable electronic equipment.

[0003]

To realize this reduction in size, reduction in thickness, and reduction in weight of portable electronic equipment, the most important issue is the improvement of the mounting density of the components.

In particular, even in semiconductor ICs and other semiconductor devices, high density mounting technology using flip-chip-type semiconductor devices instead of the package-type semiconductor devices of the related art is being developed and put into practical use.

[0004]

One of the mounting methods for mounting such a

flip-chip type semiconductor device (flip-chip mounting) is the method of forming, for example, solder ball bumps on electrode pads comprised of aluminum (Al) etc. of a semiconductor IC and bringing the connection terminals of a chip in the semiconductor IC into contact with the solder ball bumps to directly mount the IC chip on a printed circuit board.

Here, as the method of forming the solder ball bumps, there is known the method of using electrolytic plating. In this case, there is the disadvantage that the thickness of the solder formed by electrolytic plating is affected by the surface conditions of the layer of material forming the underlayer of the bumps or the slight variation in the electrical resistance and that the formation of uniform solder ball bumps of the same height in an IC chip is extremely difficult.

[0005]

On the other hand, as the method of forming the solder ball bumps of suppressing a variation of a height of the solder ball bumps, there is a method of using a pattern formation applying a film formation by vacuum deposition and lift-off of a photo resist film.

This method is performed, for example, as shown in FIG. 4.

[0006]

First, as shown in FIG. 4(a), flip-chip type semiconductor IC 1 has an electrode portion 1a formed as below.

Namely, the electrode portion 1a has electrode pads 3 comprised of an aluminum (Al) and copper (Cu) alloy etc. being formed by patterning on a semiconductor wafer 2 of silicon etc. and then by etching, a surface protective film 4 comprised of, for example, a silicon nitride film or polyimide layer etc. being formed on top of the electrode pads 3 so as to cover the entire surface of the semiconductor substrate 2, an aperture 4a formed in a region of the electrode pads 3 of the surface protective film 4, and a metal stacked film, namely, BLM (ball limiting metal) film 5, comprised of, for example, chrome, copper, and gold and formed by the sputtering method so as to cover the surface of the electrode pads 3 exposed at a side surface and a bottom portion of the aperture 4a.

[0007]

To form solder ball bumps in the electrode portion 1a of the semiconductor IC having this configuration, as shown in FIG. 4(b), a resist film 6 having an aperture 6a is formed at a region in the BLM film 5.

Then, as shown in FIG. 4(c), solder deposition films 7 are formed on the resist film 6 over the entire surface of the semiconductor substrate 2.

Then, as shown in FIG. 4(d), unnecessary portion of the solder deposition films 7 are removed by removing the resist film R2 by lift-off to form the solder deposition layers having a desired pattern.

Finally, as shown in FIG. 4(e), heat treatment is performed to make solder of the solder deposition films 7 melt to thereby form solder ball bumps 7a having spherically shaped due to the surface tension.

[0008]

Here, in general, the solder ball bumps 7a are formed in the semiconductor wafer state (that is, the state before being cut into individual semiconductor chips) of the semiconductor IC 1.

The semiconductor IC 1 formed with the solder ball bumps 7a in the electrode portion 1a in this way is cut by dicing etc. into individual chip-shaped semiconductor IC 1 from the wafer-shaped semiconductor substrate 2, then, as shown in FIG. 5, the solder ball bumps 7a in each of the semiconductor IC 1 are made to abut against the lands 8 comprised of Cu etc. serving as connecting points formed on the printed circuit board 8.

Here, the printed circuit board 8 is covered by a solder resist 8b over its entire front surface except for the lands 8a and is precoated by a eutectic solder layer 8c over the areas of the lands 8a.

Therefore, using a reflow step, the eutectic solder 8c is melted and the melted eutectic solder enters between the solder ball bumps 7a and lands 8a. By cooling and hardening it, the solder ball bumps 7a are soldered and electrically connected to the lands 8a.

[0009]

On the other hand, the joint by the solder bumps of the solder ball bumps 7a and the land 8a suffers a thermal stress in changing temperature of the surround due to the differences in the coefficients of heat expansion of the semiconductor substrate 2 and the printed circuit board 8 in the semiconductor IC 1.

Namely, while the coefficient of heat expansion of silicon comprised of the semiconductor substrate 2 is 3.4 ppm/°C, the coefficient of heat expansion of the glass epoxy-based mounting board generally widely used as the printed circuit substrate 8 is a large about 15 ppm/°C. Therefore, when thermal stress is repeatedly applied to bump joints of the solder ball bump 7a and the land 8a by the temperature difference caused by the on/off operation of the semiconductor IC 1, cracks are caused in the joints, electrically connection is cut and breakage or malfunctions are caused in some cases, namely, there is disadvantages in the reliability of the solder joints.

[0010]

To suppress the breakage of the solder joints due to the thermal stress, as shown in FIG. 5, the method is generally adopted of injecting a sealing resin 9 between the semiconductor IC 1 and the printed circuit board 8 and relieving the thermal stress applied to the bump joints by having the stress of heat expansion received by the sealing resin 9 as a whole to improve strength against to the thermal stress.

[0011]

[Problem to be Solved by the Invention]

In the configuration used with the sealing resin 9 described above, however, since the semiconductor IC 1 is integrally secured by a sealing resin in the printed circuit board 8, when a defect occurs in the semiconductor IC 1, the only method was to replace discard the entire printed circuit board 8 on which that semiconductor IC 1 was mounted and discard a defective component or apply a chemical or mechanical external force to forcibly tear the semiconductor IC 1 from printed circuit board 8.

[0012]

Here, the replacement of the entire printed circuit board 8 of the former case has the disadvantage of the cost ending up higher, while the forcibly tearing off of the semiconductor IC 1 of the latter case ends up

damaging the printed circuit board 8.

Therefore, the work of replacing a defective component in the case of a defect occurring in a semiconductor IC 1, that is, the so-called rework, is difficult. This has become one factor behind the failure of flip-chip mounting from spreading widely.

Further, along with the reduction of pitch accompanying the reduction of size of semiconductor devices, at the time of injection of the sealing resin 9, the circulation of the sealing resin 9 becomes poor and full injection of the sealing resin 9 can no longer be achieved, so there is also the disadvantage that the thermal stress cannot be sufficiently relieved.

[0013]

An object of the present invention is to provide solder bumps and a method of producing the same which enable the thermal stress between a semiconductor device and a printed circuit board to be reliably relieved without the use of a sealing resin and further which can reduce the connection resistance and can increase the strength of the joint portions.

[0014]

[Means for Solving the Problem]

The above object, according to claim 1 of the present invention, is achieved by solder bumps having

solder ball bumps formed on electrode pads of a semiconductor device and a resin filled on a surface of the pad side of the semiconductor device so as to surround a side surface of the solder ball bumps, surfaces of the solder ball bumps projecting out from the resin being cleaned by plasma cleaning.

[0015]

Further, claim 2 of the present invention is characterized in that the solder ball bumps are first solder ball bumps and the second solder ball bumps different composition from the first solder ball bumps and to be brought into contact with solder precoated to a connecting land of a printed circuit board is included on the first solder ball bumps at least in a vertical direction of the electrode pad.

[0016]

The above object, according an configuration of claim 4, is achieved by a method of producing solder bumps having: a first step of forming solder ball bumps on an electric pad of a semiconductor device; a second step of filling a resin on a surface of said pad side of said semiconductor device so as to surround a side surface of said solder ball bumps; and a third step of cleaning the surfaces of said solder ball bumps projecting out from the resin by plasma cleaning.

[0017]

According to the configuration of claims 1 or 4, the areas around the bases of the relatively weak strength solder ball bumps, namely, the areas around the first solder ball bumps, are reinforced by a resin. So the thermal stress is relieved by this resin.

Further, since the resin film is filled before the semiconductor device is mounted on the printed circuit board, so there is no need to inject the sealing resin between the printed circuit board and the semiconductor device after mounting the semiconductor device and therefore the productivity is improved. As a result, the resin is not contact to the printed circuit board, it becomes possible to easily remove the semiconductor device from the printed circuit board even if a defect occurs in a semiconductor device after mounting.

[0018]

Further, according to the configuration of claim 2, the exposed surfaces of the first solder ball bumps projecting out from the resin film are cleaned by plasma cleaning. Therefore, the connection resistance is reduced and the joint strength increased when joining the first solder ball bumps to the lands of the printed circuit board or to the second solder ball bumps.

As a result, the thermal stress is relieved when

mounting the semiconductor device to the printed circuit board, the electrical characteristics are improved and the joint strength is increased when the semiconductor device is mounted to the printed circuit board, and thereby mounting defects are reduced to a large extent.

[0019]

Further, according to the configuration of claim 5, when the plasma cleaning in the third step is at least sputter etching by a discharge plasma of an inert gas, by performing the sputter etching by RF discharge plasma using for example Ar or another inert gas, the resin remaining on the surfaces of the first solder ball bumps is removed by the sputtering and clean surfaces of the first solder ball bumps are exposed. Further, physical ion irradiation is used to chemically activate the surface layers.

As a result, the surfaces of the first solder ball bumps are cleaned, the connection resistance at the time of joining them is reduced, and the joint strength is increased, so the electrical characteristics when mounting a semiconductor device are improved.

[0020]

According to the configuration of claim 6, when the plasma cleaning in the third step is at least oxygen plasma treatment and sputter etching by discharge plasma

of an inert gas, first oxygen plasma is used to burn off the resin remaining on the surfaces of the first solder ball bumps by a reaction system comprised mainly of a combustion reaction of the organic matter mainly comprising the resin and then using RF discharge plasma using Ar or another inert gas for sputter etching and removal of the resin remaining on the surfaces of the first solder ball bumps by sputtering.

[0021]

In this case, compared with cleaning by only discharge plasma of an inert gas, two-stage plasma cleaning enables the residual resin to be effectively removed by use of a chemical reaction (combustion reaction).

Further, the slight oxide films formed on the surfaces of the first solder ball bumps during the cleaning by the oxygen plasma treatment are removed by the Ar ions by sputtering.

As a result, the surfaces of the first solder ball bumps are cleaned more, the connection resistance at the time of joining is reduced more and the joint strength is increased more.

[0022]

Further, according to the configuration of claim 7, when the plasma cleaning treatment in the third step is

at least oxygen plasma treatment and then sputter etching by discharge plasma of a reducing gas, first oxygen plasma is used to burn off the resin remaining on the surfaces of the first solder ball bumps, then HF or another reducing gas is used for sputter etching to more thoroughly remove the resin remaining on the surfaces of the first solder ball bumps.

[0023]

As a result, the surfaces of the first solder ball bumps are cleaned more, the connection resistance at the time of joining is reduced more, and the joint strength is increased more. Compared with the case of plasma cleaning by only discharge plasma of an inert gas or by discharge plasma by oxygen plasma and inert gas, the electrical characteristics at the time of mounting of the semiconductor device are improved more.

[0024]

According to claim 8, after the third step, when the forth step of forming the second solder ball bumps, which are: preferably comprised of eutectic solder; different in composition from the first solder ball bumps preferably comprised of high melting solder; and brought into contact with eutectic solder precoated to a connecting land of a printed circuit board, on the surfaces of the first solder ball bumps at least in a

vertical direction of the electrode pad is included, a portion to be core of the solder bumps is formed by the first solder ball bumps comprised of a highly elastic high melting point solder, so the thermal stress is relieved by the elastic deformation of the above high melting point solder even if the thermal stress occurs caused by the difference in coefficients of heat expansion between a silicon chip constituting the semiconductor substrate of the semiconductor device and the printed circuit board.

[0025]

Further, according to the configuration of claim 9, a portion to be brought into contact with a eutectic solder precoated to a connection lands of the printed circuit board is formed by the second solder ball bumps of a eutectic solder, the wettability with the eutectic solder precoated on the connection lands becomes excellent and reliable joining by soldering is achieved.

Further, since the surfaces of the first solder ball bumps are cleaned by the plasma cleaning, the connection resistance is reduced and the joint strength is increased at the joint portions of the first and second solder ball bumps.

Therefore, in the mounting a semiconductor device on the printed circuit board, the thermal stress is

relieved, the connection resistance is reduced and joint strength increased, whereby mounting defects are greatly reduced and the reliability of the joint portions by the metal bumps is improved.

[0026]

According to the configuration of claim 10, since the formation of the first solder ball bumps and the filling of the resin film and the plasma cleaning and, in some cases, the formation of the second solder ball bumps are performed on a semiconductor wafer when at least three steps up to the third step are performed on a semiconductor device formed on a semiconductor substrate in the semiconductor wafer state, there is no need to perform this work on the individual semiconductor devices, it is possible to perform this work on a large number of semiconductor devices at one time, and the productivity is improved more.

[0027]

[Embodiments of the Invention]

Below, preferred embodiments of the present invention will be explained in detail with reference to FIG. 1 to FIG. 3.

Note that, the embodiments given below are preferred specific examples of the present invention, so technically preferable limitations are applied to them,

but the scope of the present invention is not limited to these embodiments so long as there is no particular express limitation of the present invention in the following description.

[0028]

FIG. 1 shows an embodiment of a method of producing a solder bumps according to the present invention.

In FIG. 1(a), a semiconductor wafer 10 is formed and arranged with a plurality of flip-chip type semiconductor ICs 11.

The flip-chip type semiconductor IC 11 has, as shown in FIG. 1(a), two electrode portions 11a, and the respective electrode portion 11a is formed by the following.

Namely, as shown in FIG. 1(a), the electrode portion 11a is provided with an electrode pad 13 comprised of an aluminum and copper alloy etc. formed by patterning and etching etc. on a semiconductor substrate 12 of silicon etc., a surface protective film 14 comprised of a silicon nitride layer or polyimide layer etc. formed on top of the electrode pad 13 so as to cover the entire surface of the semiconductor substrate 12, an aperture 14a formed in a region of the electrode pad 13 of the surface protective film 14, a metal-stacked film, for example, of chrome, copper, and gold etc., namely,

BLM film 15, formed by spattering so as to cover the surface of the electrode pad 13 exposed at a side surface and a bottom portion of the aperture 14a, and a polyimide film 16 formed on the entire surface thereof so as to have the aperture 16a in the region of the BLM film 15.

[0029]

In the respective electrode portion 11a of the semiconductor ICs 11 in the semiconductor wafer 10 having this configuration, first, in the same way as the solder ball bump 7a shown in FIG. 4, the spherically shaped first solder ball bump 20 comprised of high melting solder is formed.

The first solder ball bumps 20 are formed on the BLM film 15 exposed from the aperture 16a of the polyimide film 16.

Here, the high melting point solder is comprised of for example 97 percent or so of Pb and 3 percent or so of Sn. It has a high melting point and a relatively high elasticity.

Then, an epoxy-based etc. resin 21 is coated by a spin coat etc. on the entire surface of the semiconductor wafer 10 to surround the first solder ball bumps 20, namely, to expose the surface in the vicinity of an upper edge in the drawings, then the coated resin is heat treated by curing at about 150°C for about 5 hours to

cure the resin 21.

At this state, on the surface of exposing the first solder ball bumps 20, the resin 21a is slightly and forcibly remained.

[0030]

Then, as shown in FIG. 18(b), the surface of the first solder ball bumps 20 projecting out from the resin 21 is treated by plasma cleaning.

Here, the plasma cleaning is performed as explained later by the plasma treatment device shown in FIG. 2 or FIG. 3 for example. Therefore, the surfaces of the first solder ball bumps 20 are sputter etched and the resin 21a remaining at the surfaces are removed.

[0031]

Then, the eutectic solder film pattern is formed by screen printing method on the top portion of the first solder ball bumps 20.

Note that, the above eutectic solder is comprised of for example 40 percent or so of Pb and 60 percent or so of Sn. Compared with the above-mentioned high melting point solder, it has a low melting point of, for example, not more than 200°C.

Heat treatment is applied at a temperature in a range where only the eutectic solder melts and the high melting point solder does not melt (for example, 200°C to

250°C), whereby the above eutectic solder film pattern melts and, as shown in FIG. 1(c), forms balls and hardens by the surface tension to form the second solder ball bump 22 and join with the first solder ball bumps 20.

As a result, solder bumps 23 of a stacked structure of the first solder ball bumps 20 and the second solder ball bump 22 are formed.

Here, the wafer shaped semiconductor substrate 12 is cut off by dicing to form the semiconductor ICs 11.

[0032]

The semiconductor IC 11 produced by the present embodiment is mounted on the printed circuit board 30 as mentioned below.

Namely, as shown in FIG. 1(d), in the flip-chip type semiconductor IC 11, the solder bumps 23 are opposed to lands 31 comprised of Cu etc. as contact portions formed on the printed circuit board 30.

Here, in the printed circuit board 30, the surface except the lands 31 is covered by the solder resist 32 and the region of the land 31 is precoated with the eutectic solder film 33.

[0033]

By approaching the semiconductor IC 11 to the printed circuit board 30, the solder bumps 23 are brought into contact with the corresponding lands 31. And by a

reflowing process, the eutectic solder film of the second solder ball bumps 22 and the eutectic solder film 33 precoated on the land 31 of the printed circuit board 30 are melted and jointed each other.

In this way, the flip-chip type semiconductor IC 11 is mounted with flip-chip on the printed circuit board 30.

[0034]

In this case, since the second solder ball bumps 22 is formed by a eutectic solder film, the wettability of the second solder ball bumps 22 and the eutectic solder film 33 prepared on the lands 31 is excellent. Therefore, the second solder ball bumps 22 and the lands 31 join strongly with each other due to their close affinity, so the soldering is reliable.

[0035]

Further, the first solder ball bumps 20 are secured and held by the resin 21. Even if thermal stress occurs between the semiconductor substrate 12 and the printed circuit board 30 due to changes in temperature of the surroundings after mounting, since the solder bumps 23 are secured by the resin 21 and the first solder ball bumps 20 have elasticity, the resin 21 as a whole receives the thermal stress and the first solder ball bumps 20 elastically deform so the thermal stress is relieved. As a result, breakage of the joint portions of

the solder bumps 23 due to thermal stress is prevented and the reliability of the solder bumps is improved.

[0036]

Further, since the resin 21 is filled on the surface of the electrode pad 13 side of the semiconductor IC 11 before mounting on the printed circuit board 30, the resin 21 never contacts the surface of the printed circuit board 30. Therefore, there is no need to inject resin 21 between the semiconductor IC 11 and the printed circuit board 30 as in the past, so even when reducing the pitch of semiconductor IC 11, since the resin 21 reliably covers the entire surface of the semiconductor IC 11, the thermal stress is reliably relieved and the durability with respect to thermal stress is improved.

[0037]

Further, the first solder ball bumps 20 are surrounded by the resin 21, then the exposed surfaces projecting out from the resin 21 are cleaned by plasma cleaning. Further, the second solder ball bumps 22 is formed on the cleaned surfaces, so the connection resistance at the interface of the first solder ball bumps 20 and the second solder ball bumps 22 is reduced and the joint strength is increased. Therefore, solder bumps 23 are comprised with lower resistances and higher joint strengths and the occurrence of mounting defects is

reduced more.

Therefore, according to the present embodiment, the electrical characteristics and the bonding strength at the interfaces are improved, whereby the reliability and durability of the semiconductor IC 11 and the various equipment in which it is installed are greatly improved.

[0038]

Here, the above-mentioned plasma cleaning will be explained is performed as shown below for example.

First, in a first embodiment of the plasma cleaning, the plasma treatment device shown in FIG. 2 is used for plasma cleaning by a discharge plasma of an inert gas, for example, argon gas.

In FIG. 2, the plasma treatment device 40 is a so-called triode type RF plasma treatment device comprised of a sealed plasma treatment chamber 41, a anode plate 42 provided at the top inside the plasma treatment chamber 41, a stage 43 serving as a cathode plate provided at the bottom, a lattice electrode 44 provided between the anode plate 42 and the stage 43, a plasma generation power source 46 connected via the connecting condenser 45 to the cathode plate 42, and a substrate bias power source 48 connected via the connecting condenser 47 to the stage 43.

[0039]

According to the plasma treatment device 40 of this configuration, a treated substrate, that is, the semiconductor wafer 10, is placed on the stage 43, a bias voltage is applied between the stage 43 and lattice electrode 44 by the substrate bias power source 48 in the state with, for example, an argon gas introduced inside as an inert gas, and the plasma generation power source 46 is used to apply a plasma source power between the anode plate 42 and the lattice electrode 44.

Therefore, a discharge plasma 49 of argon gas is produced between the anode plate 42 and the lattice electrode 44, and argon ions Ar^+ fly out from the anode plate 42 toward the lattice electrode 44, pass through the lattice electrode 44, and strike the semiconductor wafer 10 on the stage 42. Therefore, due to the sputtering action, the surface of the semiconductor wafer 10, that is, the surface of the resin 21 and the projecting surfaces of the first solder ball bumps 20 are etched, whereby the resin 21a remaining on the surfaces of the first solder ball bumps 20 is removed.

[0040]

In this case, the operating conditions of the above plasma treatment device 40 are set as shown below for example. That is,

Flow rate of argon gas: 25 sccm

Temperature of stage 43: Room temperature

Plasma source power: 700W (2 MHZ)

Substrate bias voltage: 350V (13.56 MHZ)

Treatment time: 120 seconds

When the plasma cleaning of the semiconductor wafer 10 was performed by these operating conditions, due to the sputtering action of the Ar^+ ions, the resin 21a remaining on the surfaces of the first solder ball bumps 20 was effectively removed and the surfaces of the first solder ball bumps 20 were cleaned.

[0041]

Next, in the second embodiment of the plasma cleaning, the plasma treatment device shown in FIG. 3 was used for oxygen plasma treatment, then discharge plasma of a reducing gas was used for plasma cleaning.

In FIG. 3, the plasma treatment device 50 is an ICP (Inductively Coupled Plasma) high density plasma treatment device of a known configuration comprised of a sealed plasma treatment chamber 51, an anode plate 52 provided at the top inside the plasma treatment chamber 51, a vertically movable stage 53 serving as a cathode plate provided at the bottom, an inductively coupled coil 54 provided around the plasma treatment chamber 51, a substrate bias power source 56 connected through a coupling capacitor 55 to the stage 53, and an ICP power

source 57 connected to the inductively coupled coil 54.

[0042]

According to the plasma treatment device 50 of this configuration, a treated substrate, that is, the semiconductor wafer 10, is placed on the stage 53, a bias voltage is applied between the stage 53 and anode plate 52 by the substrate bias power source 56 in the state with oxygen gas introduced inside, and a high frequency induction field is produced inside the plasma treatment chamber 51.

Therefore, the electrons inside the plasma treatment chamber 51 are accelerated, a high density oxygen plasma 58 is produced, and oxygen ions strike the semiconductor wafer 10 on the stage 52. Therefore, due to the plasma ashing action, the surface of the semiconductor wafer 10, that is, the surface of the resin 21 and the projecting surfaces of the first solder ball bumps 20, are etched, whereby the resin 21a remaining on the surfaces of the first solder ball bumps 20 are removed.

[0043]

In this case, the operating conditions of the above plasma treatment device 50 are set as shown below for example. That is,

Flow rate of oxygen gas: 50 sccm

Pressure: 0.3 Pa

Temperature of stage 53: 90°C

Power of ICP power source: 1000W (450 kHz)

Substrate bias voltage: 100V (13.56 MHZ)

Treatment time: 20 seconds

When the plasma cleaning of the semiconductor wafer 10 was performed by these operating conditions, due to the ashing action of the oxygen plasma, the resin 21a remaining on the surfaces of the first solder ball bumps 20 was effectively removed.

Note that, in this case, the surfaces of the first solder ball bumps 20 are slightly oxidized by the oxygen plasma and an oxide film is formed.

[0044]

Then, plasma etching is performed by reducing gas to remove the oxide film of the surface of the first solder ball bumps 20.

This reducing gas plasma etching is performed in the above plasma treatment device 50 by changing the settings of the operating conditions, introducing a mixed gas of, for example, hydrofluoride (HF) gas as the reducing gas and, for example, argon gas as the inert gas inside the plasma treatment chamber 51, and etching the surfaces of the first solder ball bumps 20 by the plasma etching action of the reducing gas.

[0045]

In this case, the operating conditions of the above plasma treatment device 50 are set as shown below for example. That is,

Flow rate of HF gas: 25 sccm

Flow rate of argon gas: 25 sccm

Pressure: 0.13 Pa

Temperature of stage 53: 90°C

Power of ICP power source: 1000W (450 kHz)

Substrate bias voltage: 250V (13.56 MHZ)

Treatment time: 20 seconds

When the plasma cleaning of the semiconductor wafer 10 is performed by these operating conditions, the oxide film formed on the surfaces of the first solder ball bumps 20 is reduced by the reaction with the HF gas and the sputtering action of the Ar^+ ions causes sputter removal and cleans the surfaces of the first solder ball bumps 20.

[0046]

In this case, a high density plasma generation source is used by the plasma treatment device 50 and treatment in a low pressure atmosphere is enabled by this. As a result, the ion species produced in large quantities strike the surface of the semiconductor wafer 10 substantially perpendicularly without scattering and the

etching by the sputtering by irradiation of Ar^+ ions is performed at a high speed with good efficiency.

Therefore, even if the substrate bias voltage is set low so as to reduce the damage caused by the plasma cleaning of the semiconductor IC 11, the time required for the plasma cleaning of the surfaces of the first solder ball bumps 20 is shortened without a reduction in the etching rate.

[0047]

Therefore, the resin 21a remaining on the surfaces of the first solder ball bumps 20 are more effectively removed by the plasma ashing by the oxygen plasma and the plasma etching by the reducing gas and the surfaces are cleaned more.

[0048]

In the above embodiments, the first solder ball bumps 20 are covered by a film by vacuum evaporation and a pattern is formed by lift-off of the photoresist, but the invention is not limited to this. It is clear that electroplating etc. may also be used to form it.

[0049]

Further, in the above embodiments, hydrofluoride gas HF was used as the reducing gas, but the invention is not limited to this. For example, it is clear that it is also possible to use for example hydrogen gas H_2 or

hydrochloride gas HCl or another reducing gas.

Here, when using a liquid form of HF or HCl etc., for example bubbling using helium He or another carrier gas, heating aeration, ultrasonic aeration, or another suitable means is used to introduce it into the plasma treatment chamber 41, 51.

[0050]

Further, in the above embodiments, a triode-type RF plasma treatment device 40 or ICP high density plasma treatment device 50 was used for the plasma cleaning of the surfaces of the first solder ball bumps 20, but the invention is not limited to this. For example, it is clear that it is also possible to use a parallel plate type RF plasma treatment device or a so-called TCP, ECR, helicon wave plasma, or other type of high density plasma treatment device.

[0051]

Further, in the above embodiment, the explanation was given of the case of forming solder bumps 23 with respect to the electrode pads 13 of the semiconductor IC 11, but the invention is not limited to this. It is clear that the present invention may also be applied to the case of forming solder bumps with respect to other types of semiconductor devices.

[0052]

[Effect of the Invention]

As mentioned above, according to the present invention, it is to provide solder bumps and a method of forming the same which enable the thermal stress between a semiconductor device and a printed circuit board to be reliably relieved without the use of a sealing resin and further which can reduce the connection resistance and can increase the strength of the joint portions.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1] FIG. 1 are schematic cross-sectional views of production steps of an embodiment of a method of forming a solder bumps according to the present invention successively.

[FIG. 2] FIG. 2 is a schematic cross-sectional view showing a first example of a configuration of a plasma treatment device for plasma cleaning in a production process of FIG. 1.

[FIG. 3] FIG. 3 is a schematic cross-sectional view showing a second example of a configuration of a plasma treatment device for plasma cleaning in the production process of FIG. 1.

[FIG. 4] FIG. 4 are cross-sectional views of steps of an example of a conventional method of producing a solder bumps.

[FIG. 5] FIG. 5 is a schematic cross-sectional view

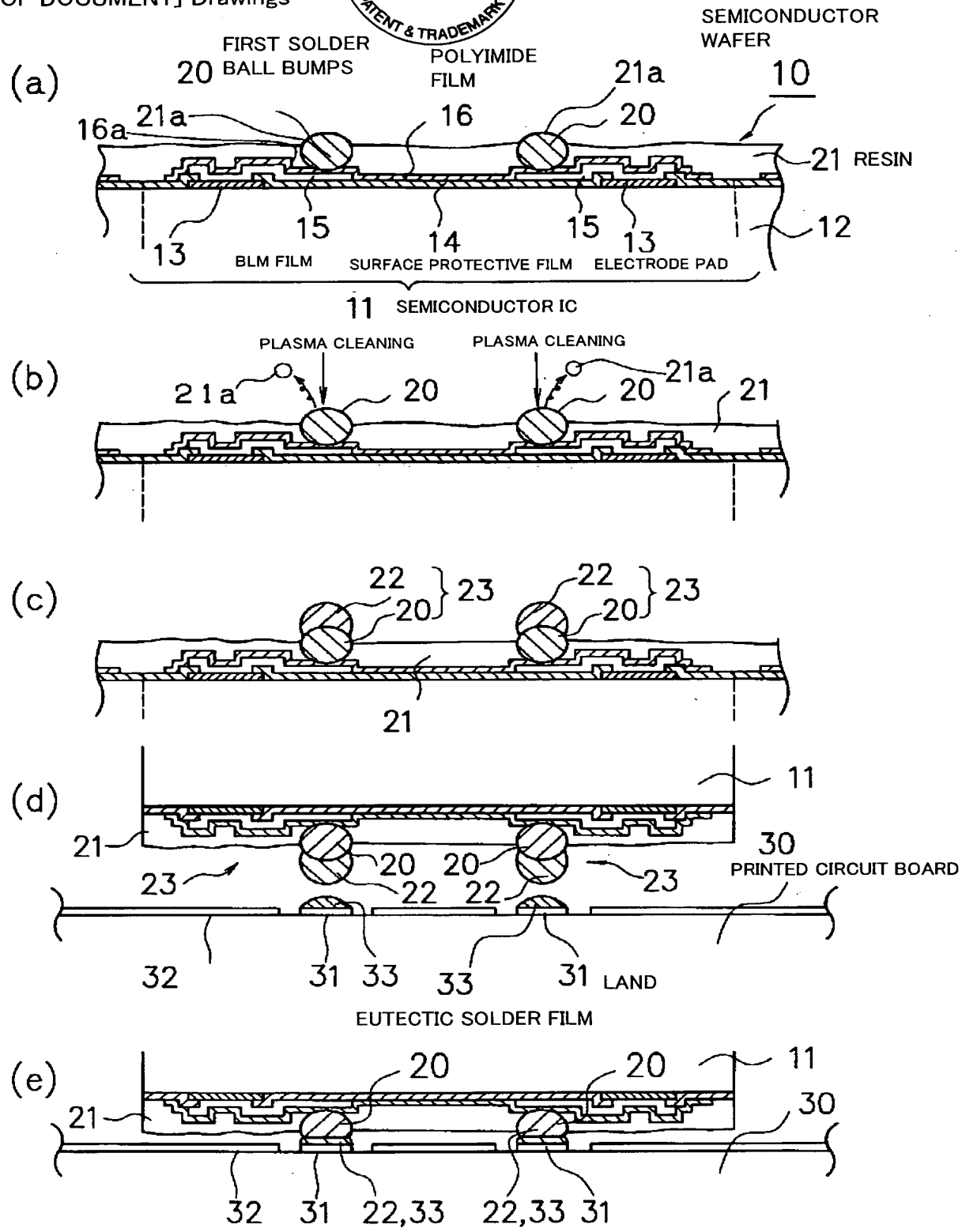
showing a mounting state of a flip-chip type semiconductor IC on a printed circuit board by using solder bumps produced by the method of producing the solder bumps in FIG. 4.

[Description of References]

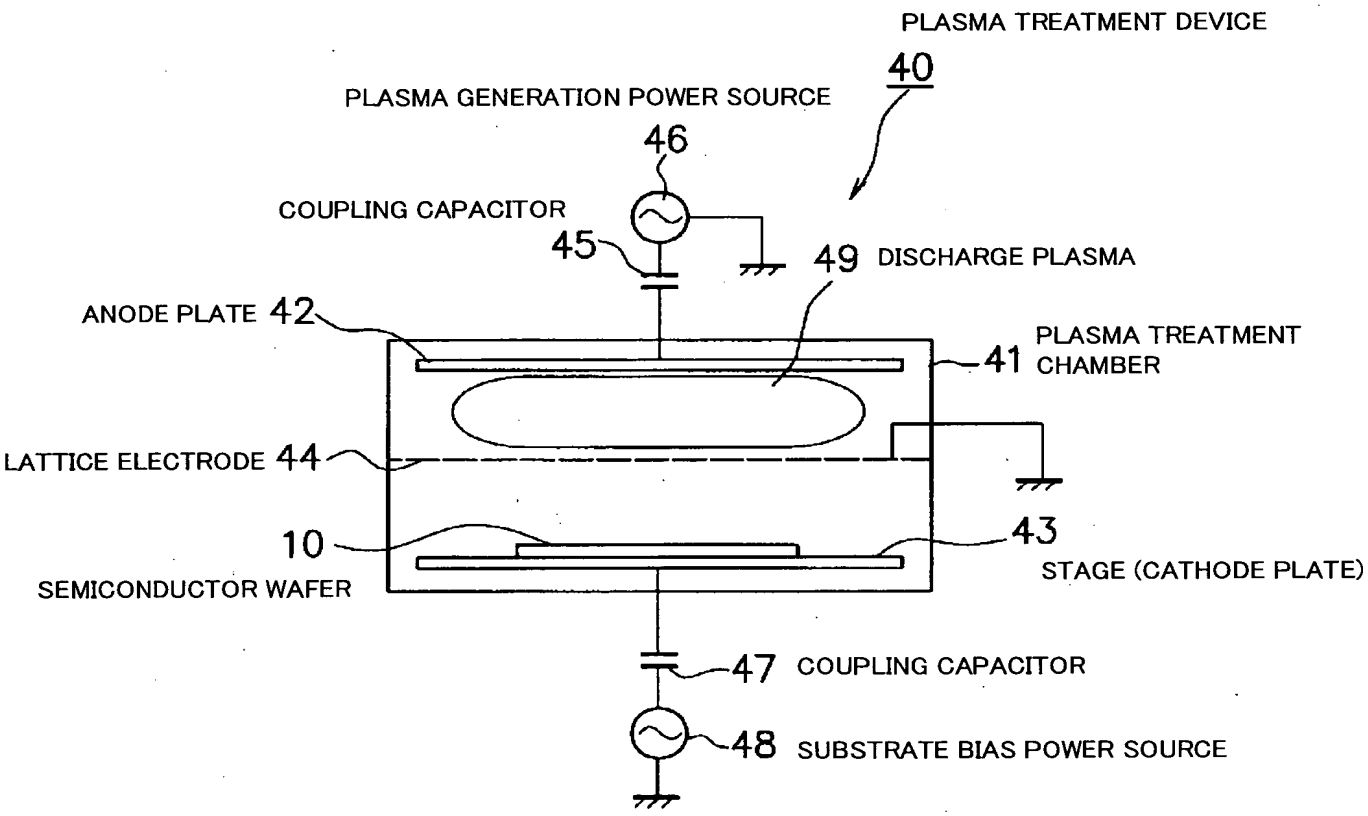
10...semiconductor wafer; 11...semiconductor IC; 12...semiconductor substrate; 13...electrode pads; 14...surface protective film; 15...BLM film; 16...polyimide film; 20...first solder ball bumps (high melting point solder); 21...resin; 22... second solder ball bumps (eutectic solder); 23...solder bumps; 30...printed circuit board; 31...lands; 32...solder resist; 33...eutectic solder film; 40...plasma treatment device (triode-type RF plasma treatment device); 41, 51...plasma treatment chamber; 42, 52...anode electrode; 43, 53...stage (cathode electrode); 44...lattice electrode; 45, 47, 55...coupling capacitor; 46...plasma generation power source; 48, 56...substrate bias power source; 49...discharge plasma; 50...plasma treatment device (ICP high density plasma treatment device); 54...inductively coupled coil; 57...ICP power source; 58....high density plasma.

[NAME OF DOCUMENT] Drawings

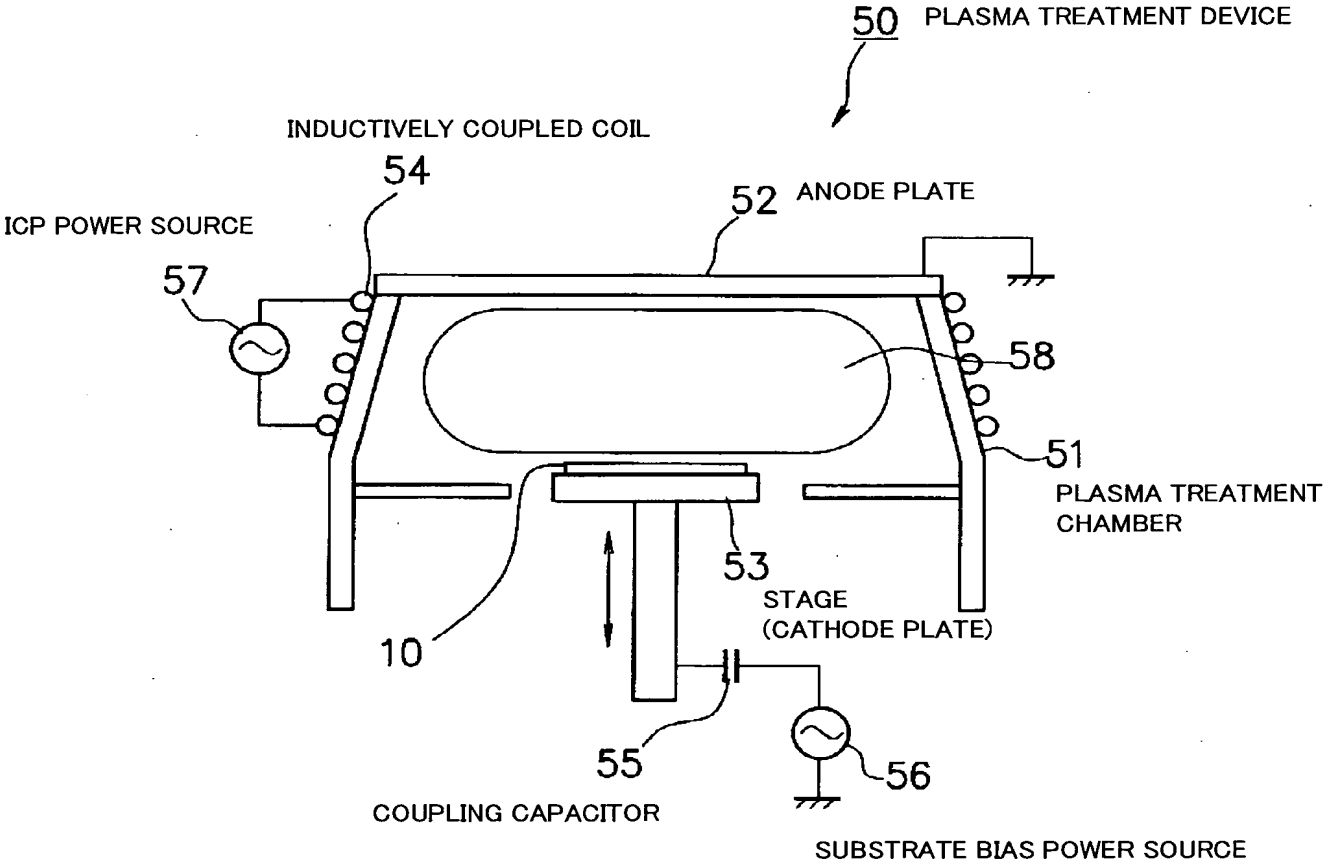
[FIG. 1]



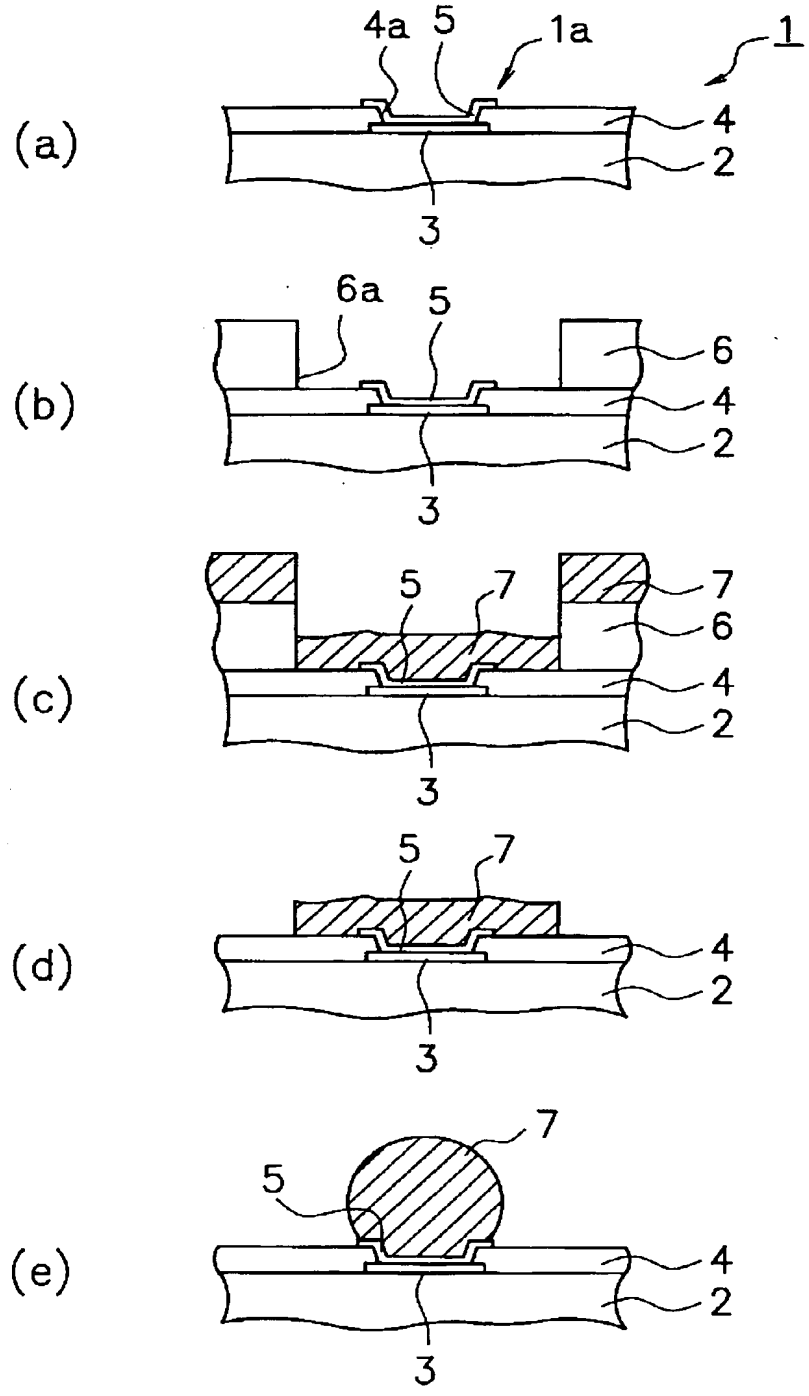
[FIG. 2]


PLASMA TREATMENT DEVICE
40
PLASMA GENERATION POWER SOURCE
46
COUPLING CAPACITOR
45
49 DISCHARGE PLASMA
ANODE PLATE 42
41 PLASMA TREATMENT CHAMBER
LATTICE ELECTRODE 44
10
SEMICONDUCTOR WAFER
43
STAGE (CATHODE PLATE)
47 COUPLING CAPACITOR
48 SUBSTRATE BIAS POWER SOURCE

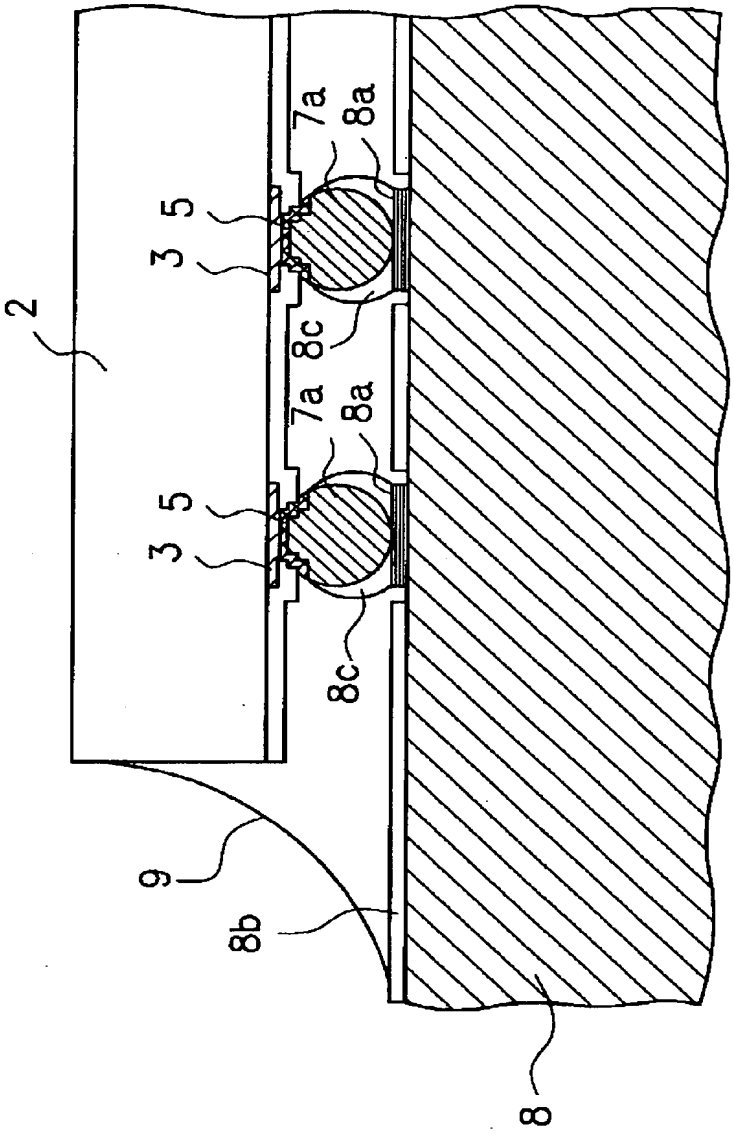
[FIG. 3]


50 PLASMA TREATMENT DEVICE
INDUCTIVELY COUPLED COIL
54
52 ANODE PLATE
ICP POWER SOURCE
57
58
51
PLASMA TREATMENT CHAMBER
53
STAGE (CATHODE PLATE)
10
55
56
COUPLING CAPACITOR
SUBSTRATE BIAS POWER SOURCE

[FIG. 4]



[FIG. 5]



[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[PROBLEM] To provide solder bumps and a method of producing the same which enable the thermal stress between a semiconductor device and a printed circuit board to be reliably relieved without the use of a sealing resin and further which can reduce the connection resistance and can increase the strength of the joint portions.

[MEANS FOR SOLUTION] A solder bumps 23 includes: first solder ball bumps 20 formed on electrode pads 13 of a semiconductor device 11; and a resin 21 filled on a surface of a pad side of the semiconductor device so as to surround a side surface of the first solder ball bumps 20, the surfaces of the first solder ball bumps projecting out from the resin being cleaned by plasma cleaning.

[SELECTED DRAWING] FIG. 1